

CLOCK AND DATA RECOVERY SYSTEM FOR A WIDE RANGE OF BIT RATES

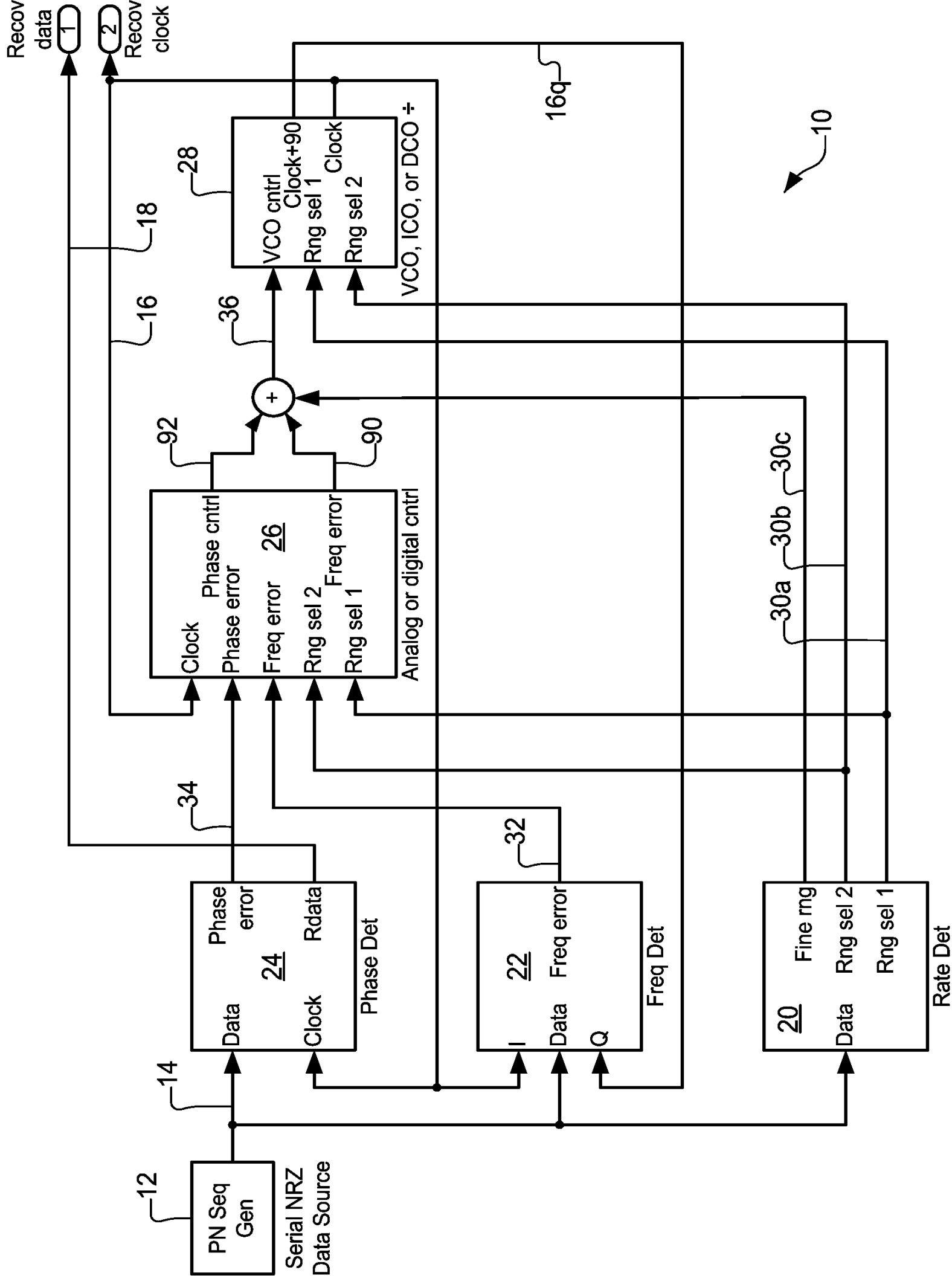
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10	CDR circuit	77	summing unit
12	data source	78a-d	flip-flops
14	source data signal	80a-b	NOT logical operators
16	recovered clock signal	82a-d	XOR logical operators
16q	shifted clock signal	84	summing unit
18	recovered data signal	86	reset unit
20	rate detector	90	frequency control signal
22	frequency detector	92	phase control signal
24	phase detector	94	integrator
26	filter-controller	96a-c	amplifiers
28	oscillator-divider	98a-b	switches
30a-c	range select signals	100a-c	zero pole filters
32	frequency error signal	102a-b	switches
34	phase error signal	104	gated integrator
36	driving signal	106	amplifier
40a-c	rate range units	108	sample and hold unit
42a-b	switches	110	frequency divider
44	input tailoring circuitry	112	filter
46	filter	120	VCO
48	output tailoring circuitry	122a-b	frequency dividers
50	transport delay	124a-b	switches
52	XOR logical operator	126	divider-phase generator
54	one-shot unit	150	receiver
56	summing unit	152	photodiode
58	level shift sub-circuitry	154	conditioning circuitry
60	buffer	156	trans-impedance amplifier
62	quantitizer	158	post amplifier
70	transport delay	160	transceiver
72	XOR logical operator	162	photodiode
74	matching circuit	164	frequency converter
76a-b	one-shot units	166	multiplexer



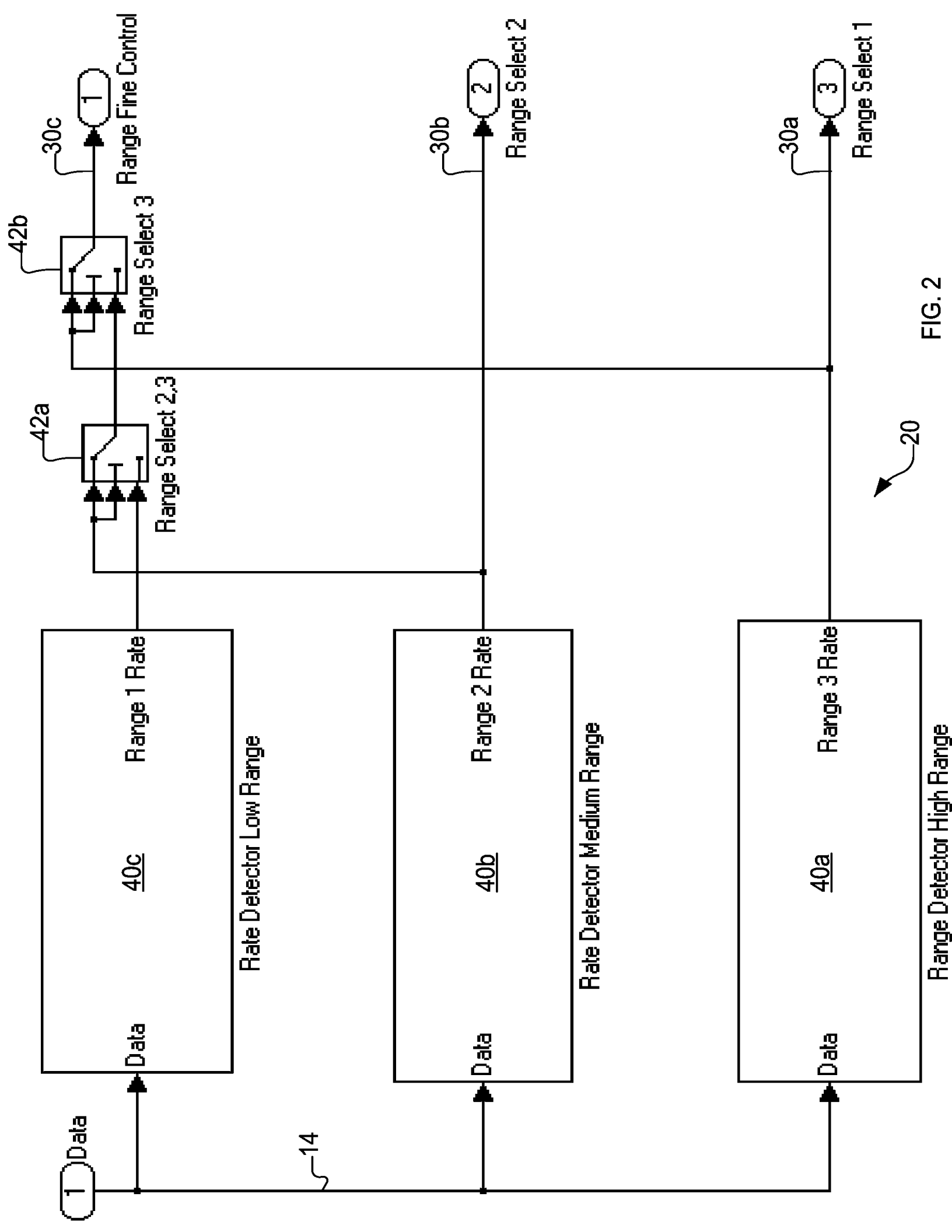


FIG. 2

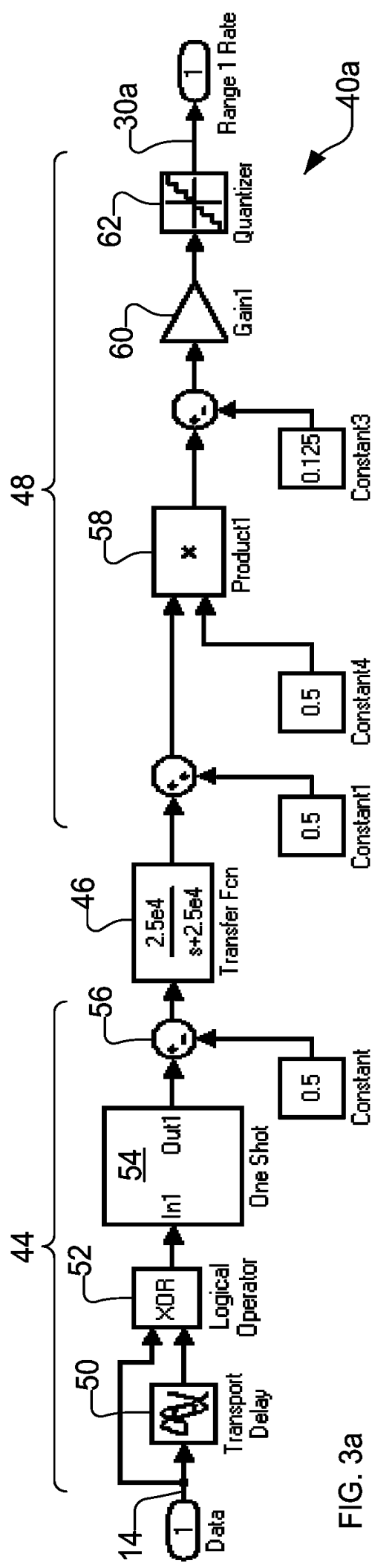


FIG. 3a

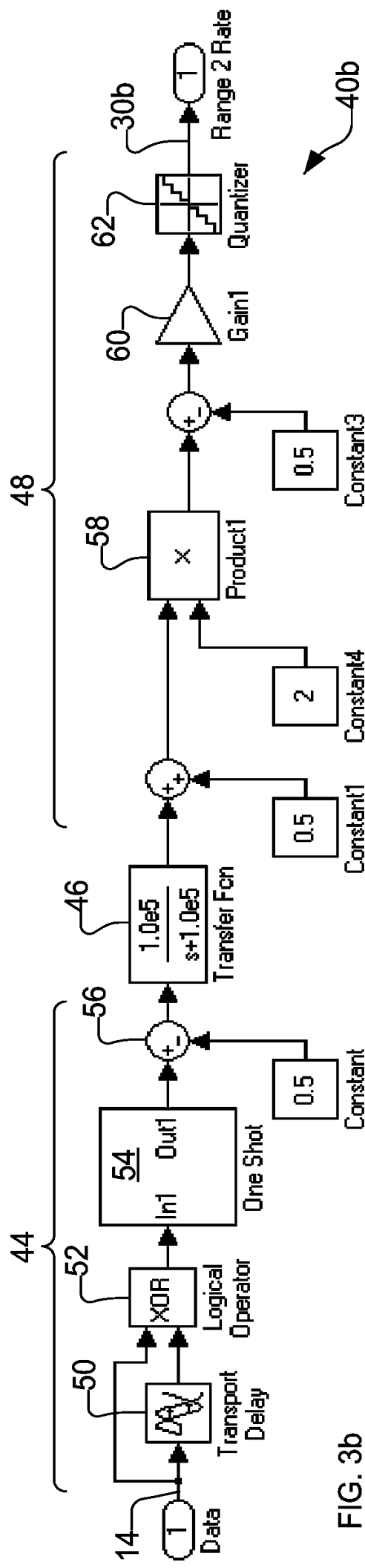


FIG. 3b

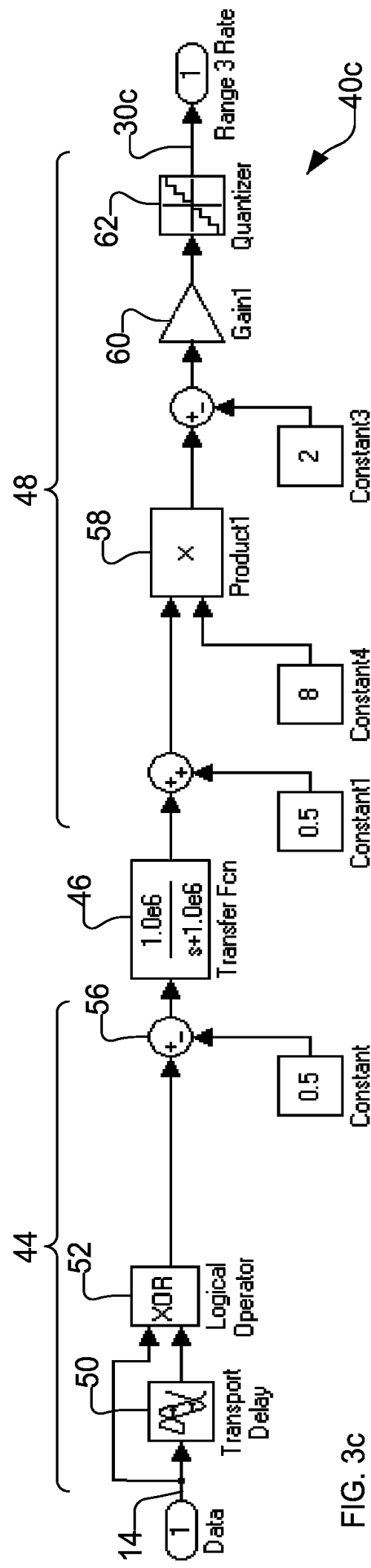


FIG. 3c

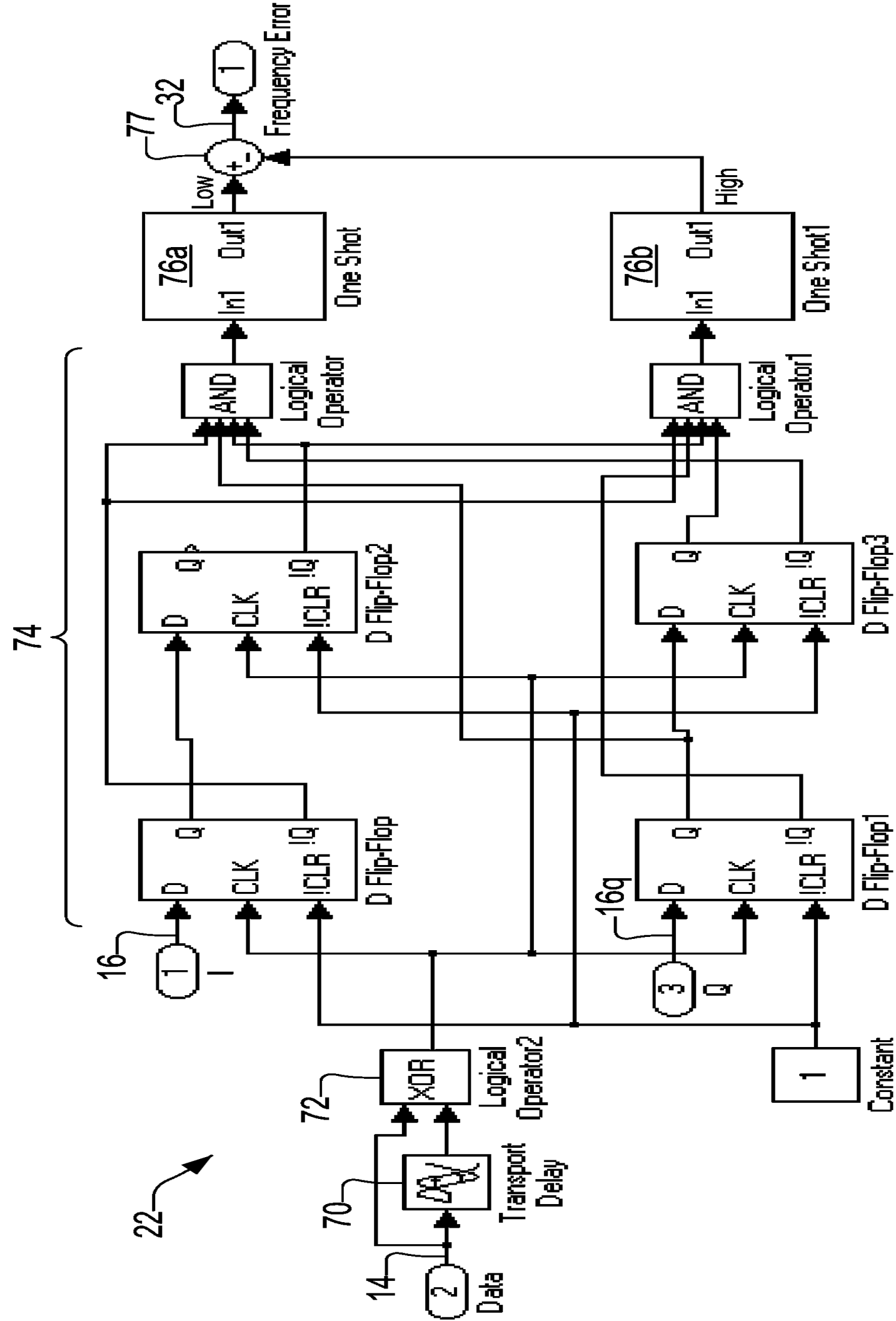


FIG. 4

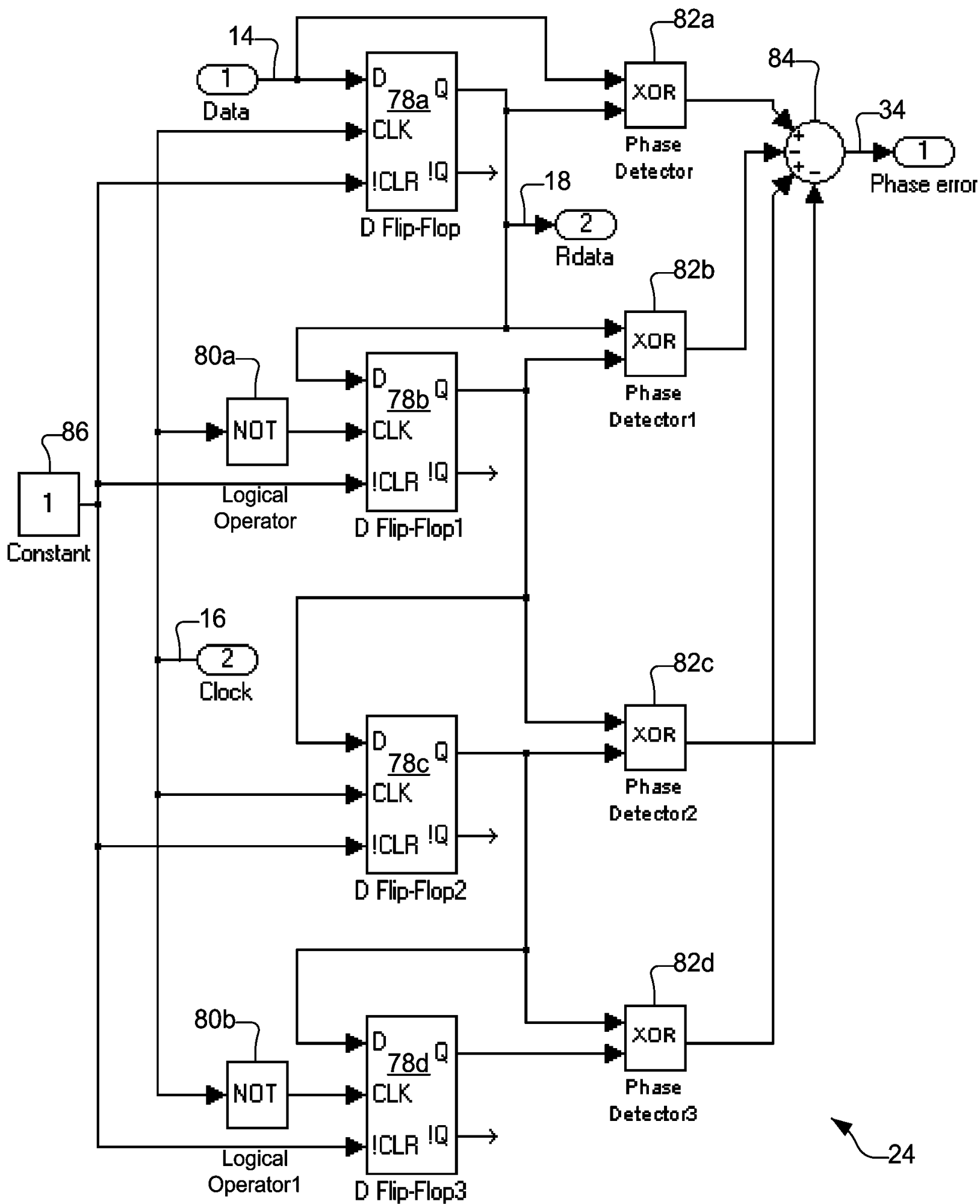


FIG. 5

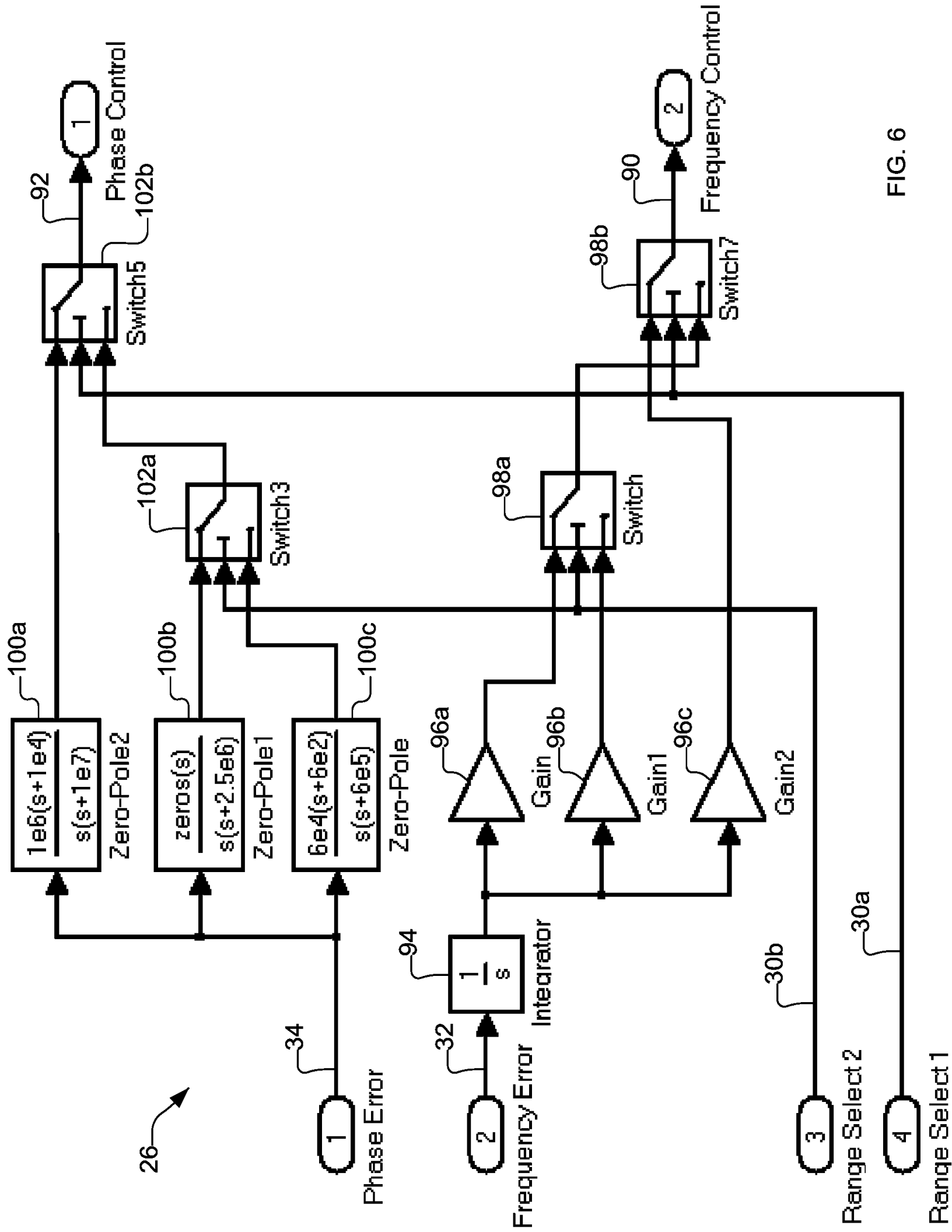


FIG. 6

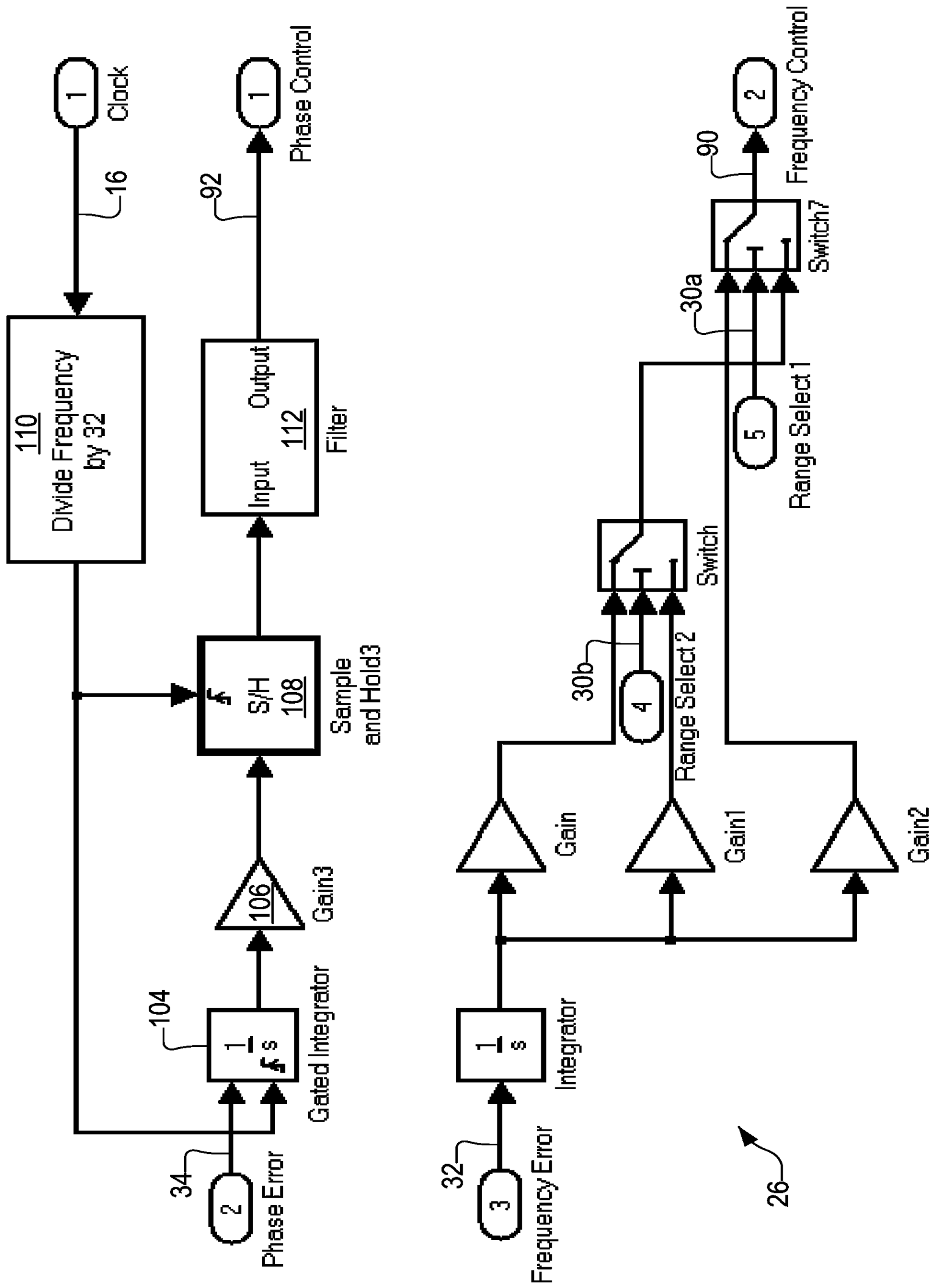


FIG. 7

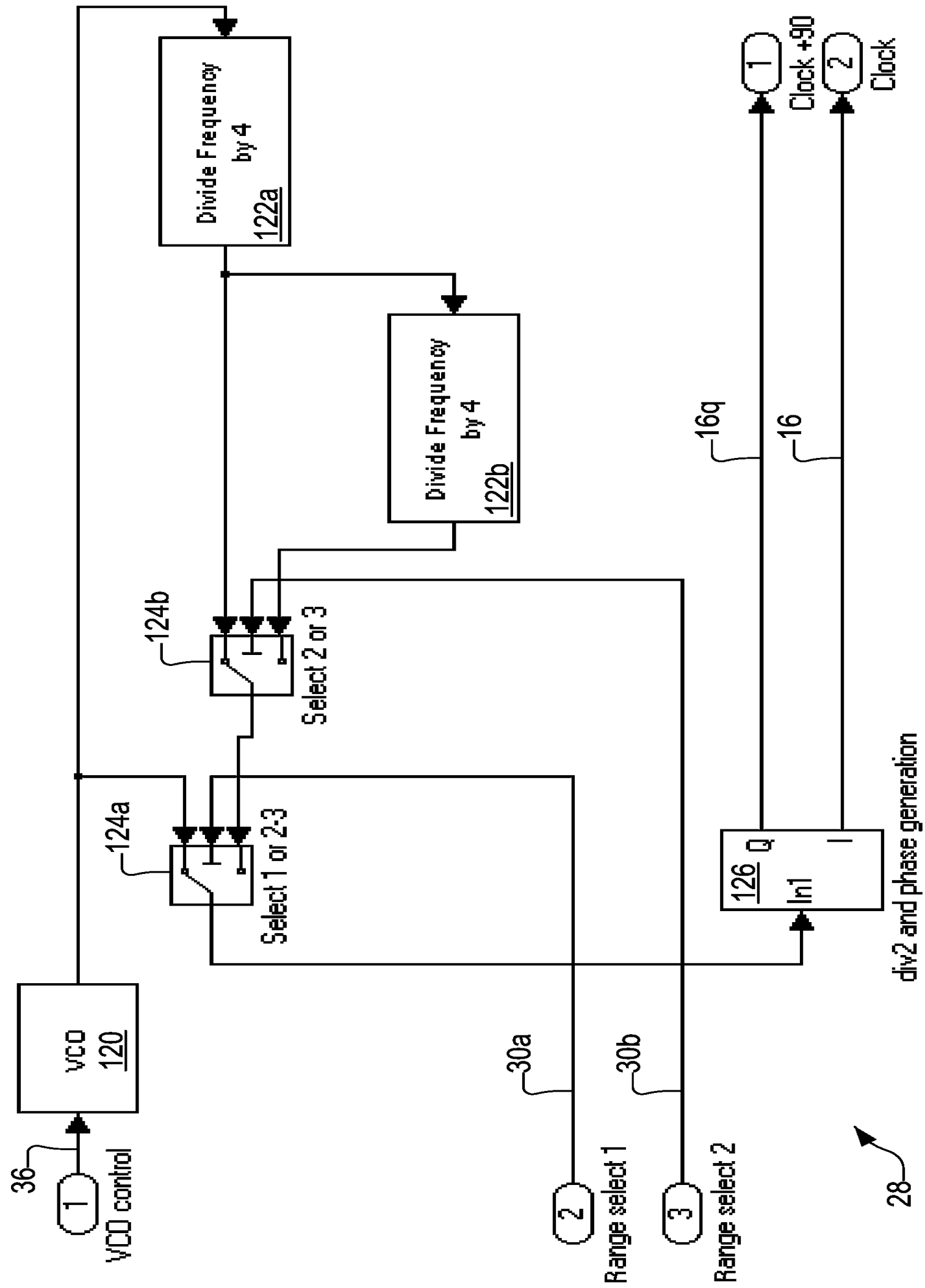


FIG. 8

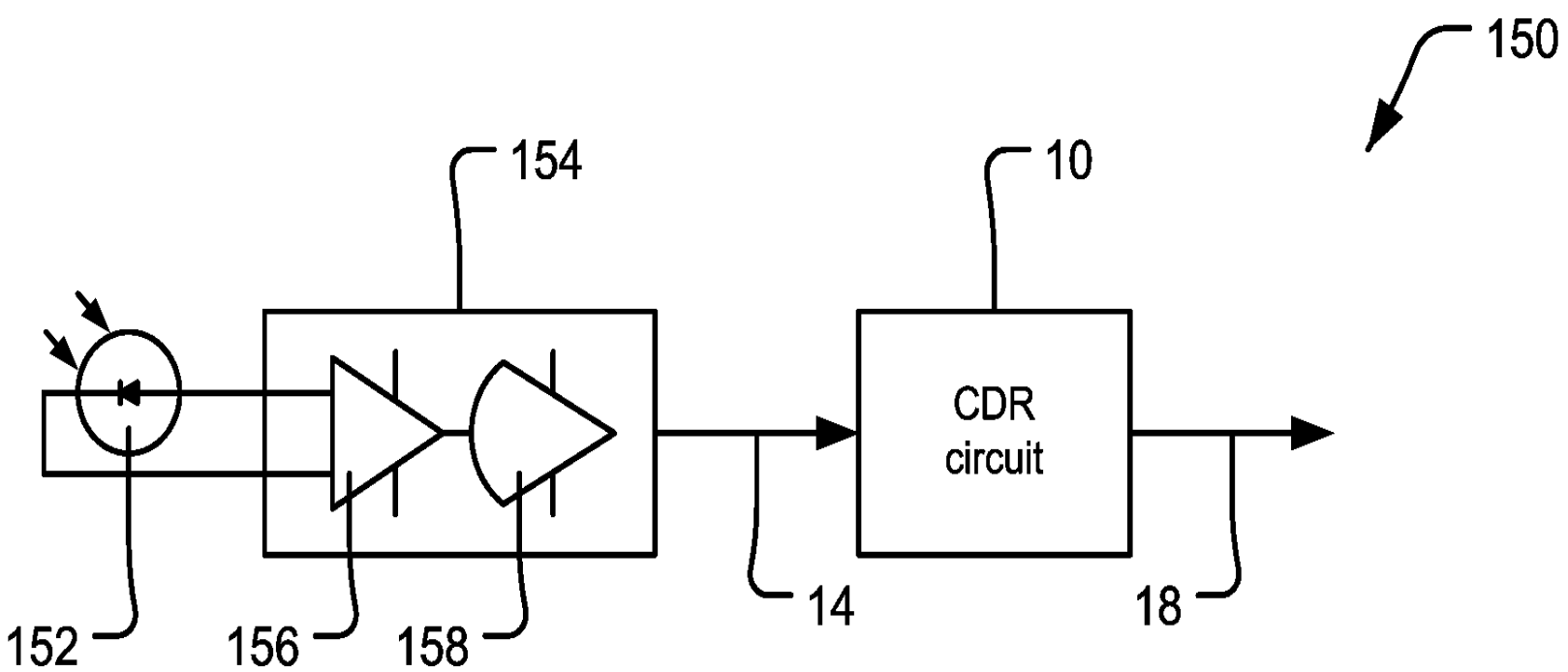


FIG. 9

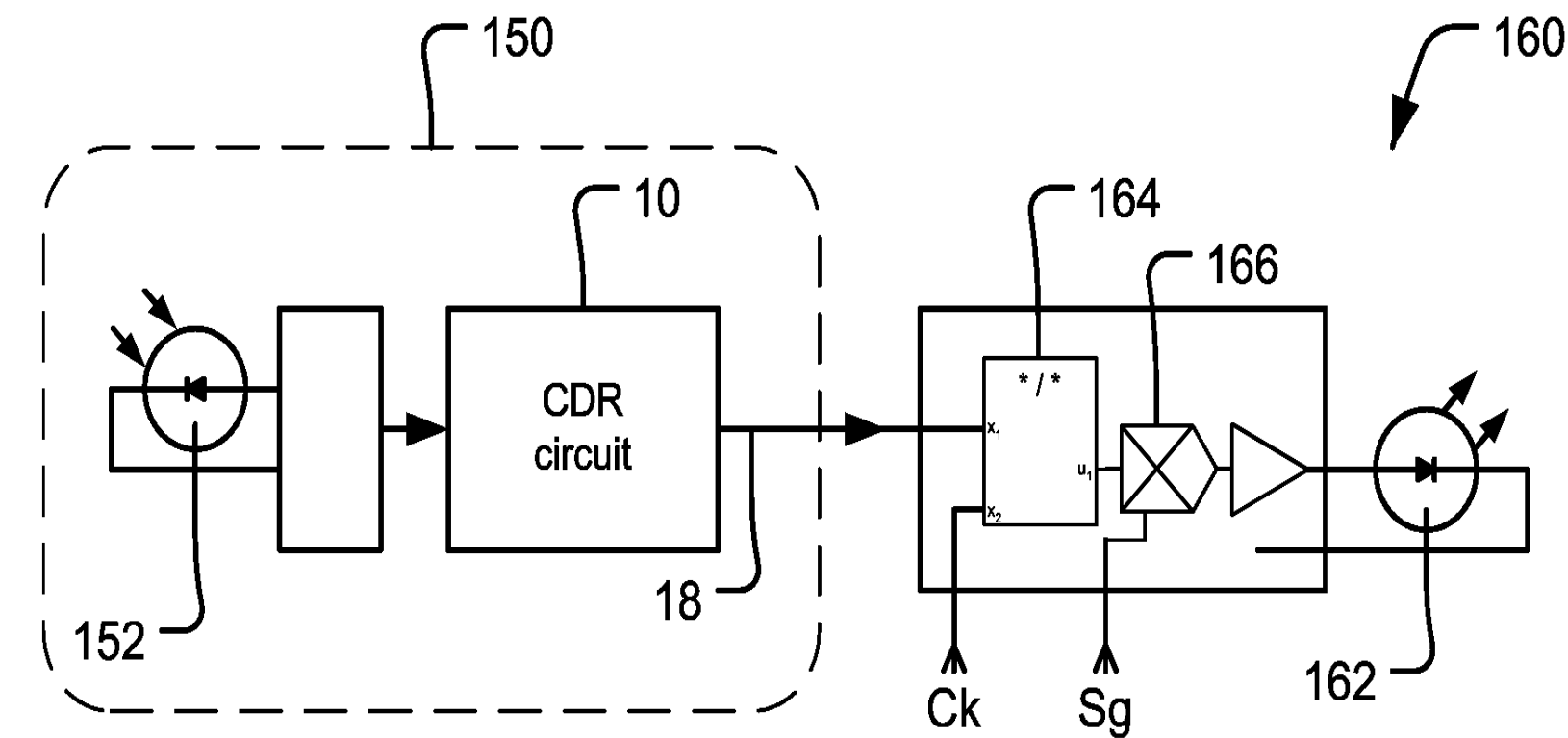


FIG. 10